REMARKS

Claims 1, 3, 4, 6, and 8 are all the claims pending in the application. By this Amendment, Applicant amends claim 1 to further clarify the invention. In addition, Applicant rewrites claim 5 into its independent form. Claim 4 is canceled.

Applicant also amends the specification to fix a minor typographical error.

I. Preliminary Matters

As preliminary matters, the Examiner's acknowledgement of the claim to foreign priority, and confirmation that the certified copy of the priority document was received is gratefully noted, and also the Examiner's initialing of the references listed on Form PTO-1449 submitted with information disclosure statement on November 29, 2001. In addition, the Examiner's acknowledgement and entry of the Preliminary Amendment filed on March 15, 2002 is noted.

II. Summary of the Office Action

Turning to the merits of the Office Action, the Examiner objected to the Drawings, and rejected claim 5 under 35 U.S.C. § 112, second paragraph, and claims 1, 3-6, and 8 under 35 U.S.C. § 103(a).

III. Objection to the Drawings

The Examiner has objected to the drawings received on March 15, 2002. In particular, the Examiner objected to the Drawings because Figures 16-24 are not labeled "Prior Art", and because Figures 20 and 23 are inconsistent with the specification at steps 211, 217, 219, 221, 243, 245, 247, and 249.

To remedy these minor informalities, Applicant labels Figures 16-24 "prior art".

Moreover, in Figures 20 and 23, Applicant amends the label "A 15:0/D 15:0 START ADDRESS OUTPUT" in step 211 to recite "A 15:2/D15:0 START ADDRESS OUTPUT" and in steps 217, 219, 221, 243, 245, 247, and 249 the label "A 2:0 SWITCH" to recite "A 1:0 SWITCH,"

In addition, for further conformity with the specification, Applicant amends Figures 1 and 16 by changing the references "..c" and "C" appearing in Figures 1 and 16 to "..n" and "N".

In view of these self-explanatory amendments to the Drawings, Applicant respectfully requests the Examiner to withdraw the objections to the Drawings and to indicate approval of the drawing corrections in the next Patent Office paper.

IV. Claim Rejections under 35 U.S.C. § 112

The Examiner rejected claim 5 under section 112, second paragraph, for improper antecedent basis. Applicant thanks the Examiner for pointing out, with particularity, the aspects of the claim thought to be indefinite. Applicant respectfully requests the Examiner to withdraw this rejection in view of the self-explanatory claim amendment being made herein.

V. Claim Rejections under 35 U.S.C. § 103

With regard to the prior art rejections, the Examiner rejected claims 1, 3-6, and 8 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter "APA") in view of Japanese Patent Publication No. 01-173149 to Oshikawa (hereinafter "Oshikawa"). Applicant respectfully traverses these rejections in view of the following comments.

In the exemplary, non-limiting embodiment of the present invention, a data transmission system that can execute continuous data transmission in fewer signal lines and without malfunctions caused by the disturbances between the control signals in the data transmission. The data transmission between the primary board and the secondary boards using the same data transmission signal line as an address bus and a data bus, mutually.

Prior art disclosed in the specification teaches that each time the direction is switched, an additional signal line carrying the lower two bits of the next address must be provided, thereby the number of data in the continuous transmission is decided by the number of lower address signal lines. Adding the lower address signal lines results in an increased cost and package size.

In the exemplary, non-limiting embodiment, however, the next transmission address is obtained by incrementing the transmission start address stored in the secondary board, therefore there is no need to read/write address every transmission operation. As a result, the continuous transmission can be accomplished using few signal lines. In addition, in the exemplary, non-limiting embodiment, a cycle signal that counts three times the leading edge of the clock to toggle is provided. That is, the secondary board does not shift to the next process until the phase has been toggled. The leading and trailing edges of the trigger detected in combination with the toggle states of the phase prevents disturbances generated on the trigger. This exemplary, non-limiting embodiment is provided by way of an example only and is not intended to limit the scope of the claims in any way.

Next, turning to the rejections, claims 1, 3-6, and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over APA in view of Oshikawa. Turning to the cited references, APA teaches transmitting lower address bits (A1:0) at each switch. Oshikawa teaches

performing the transfer of data at a high speed by producing automatically a series of addresses which are necessary for accesses to all access areas desired by an application module within a memory module based on the head address of a relevant area.

In particular, Oshikawa teaches an address buffer containing a counter function which is used together with a bus interface which controls a swap means. Then a series of addresses which are necessary for accesses to all access areas are successively produced by the buffer 44 under the control of the interface. An application module is not required to deliver said series of addresses after the output of the head address of a desired access area and therefore can use an address/data line only for transfer of the read data. As a result, data can be transferred at a high speed compared with a conventional case where the address/data line is used alternately for transfer of the read address received from the application module and the data received from a memory module.

Claim 4 is canceled. Therefore, this rejection with respect to claim 4 is literally moot. Of the remaining rejected claims, only claims 1, 5, 6, and 8 are independent. The Examiner contends that APA and Oshikawa suggest each feature of the independent claims. The Examiner acknowledges that APA does not teach or suggest generating an address, where the cycle signal is used in combination with the trigger signal (see pages 4-6 of the Office Action).

In particular, the Examiner acknowledges that APA does not teach or suggest "generating an address used in the data access in the secondary boards based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger signal," as recited in claim 1, "generating an address, to which the data transmission is subsequently executed, in the secondary boards by incrementing the memory

start address after the data transmission based on the memory start address is ended, and then executing the data transmission via the data transmission path by accessing the memory of own station based on the generated address, wherein a cycle signal indicating switching of data is used in combination with a trigger signal" as recited in claim 5, "informing a trigger signal combined with a cycle signal indicating a timing of data access, and a start address required for data read via the data transmission path,...incrementing the start address at a timing of the trigger signal," as recited in claim 6, and "informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,... incrementing the start address at a timing of the trigger signal," as recited in claim 8.

The Examiner, however, alleges that Oshikawa cures the deficient teachings of the APA. In particular, the Examiner alleges that Oshikawa's memory address, counter for a predetermined byte transfer, and data enable signal are combined to access memory data and are equivalent to generating an address used in the data access in the secondary board based on the start address, a predetermined trigger signal and a cycle signal combined with the trigger signal (see pages 4-5 of the Office Action). Applicant respectfully disagrees.

Oshikawa teaches incrementing the address using the count signal and the data enable. In Oshikawa, however, there is a possibility that the address is erroneously incremented due to the deformation of the wave of the count signal during data enabling, which is caused by external noise or signal reflection. In other words, Oshikawa fails to teach or suggest not incrementing or generating an address during the time in which the waveform is deformed by the count signal or noise. That is, Oshikawa fails to teach or suggest using a cycle signal indicating the switching of

data in combination with the trigger signal. In Oshikawa, there is no cycle signal used in combination with the trigger signal that would indicate the switching to the previous data while alternating L/H for each switching of data. As a result, Oshikawa cannot prevent the occurrence of erroneous count up of the address when noise or reflection is overlapped on the count signal. In short, Oshikawa fails to teach or suggest generating an address based on the trigger signal combined with a cycle signal that indicates switching of data. Oshikawa does not cure the deficient teachings of the APA.

Therefore, "generating an address used in the data access in the secondary boards based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger signal," as recited in claim 1, "generating an address, to which the data transmission is subsequently executed, in the secondary boards by incrementing the memory start address after the data transmission based on the memory start address is ended, and then executing the data transmission via the data transmission path by accessing the memory of own station based on the generated address, wherein a cycle signal indicating switching of data is used in combination with a trigger signal" as recited in claim 5, "informing a trigger signal combined with a cycle signal indicating a timing of data access, and a start address required for data read via the data transmission path,...incrementing the start address at a timing of the trigger signal," as recited in claim 6, and "informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,... incrementing the start address at a timing of the trigger signal," as recited in claim 8, is not suggested or taught by the combined teachings of

APA and Oshikawa, which lack generating or incrementing an address based on a trigger signal combined with a cycle signal that indicates the switching of data.

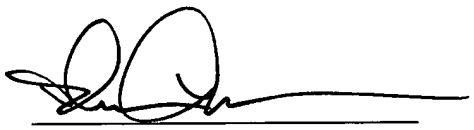
For at least these exemplary reasons, Applicant respectfully requests the Examiner to withdraw this rejection of claims 1, 5, 6, and 8. Claim 3 is patentable at least by virtue of its dependency on claim 1.

VI. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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AMENDMENTS TO THE DRAWINGS

The attached seven (7) sheets of drawings includes the following changes:

In Figures 1 and 16, reference "..c" and "C" are changed to "..n" and "N".

In Figures 16-24, the "Prior Art" label is added.

In Figures 20 and 23 changing "A 15:0/D 15:0 START ADDRESS OUTPUT" in step 211 to "A 15:2/D15:0 START ADDRESS OUTPUT" and in steps 217, 219, 221, 243, 245, 247, and 249 changing "A 2:0 SWITCH" to "A 1:0 SWITCH,"

Attachment: Annotated Marked-Up Drawings (7 sheets)